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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,491	06/20/2003	Frank Sacca	0120104C	9887

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EXAMINER	
SWERDLOW, DANIEL	

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 08/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,491	SACCA ET AL.	
	Examiner	Art Unit	
	Daniel Swerdlow	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/20/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the connection of the base of the electronic inductor transistor to ground when the telephone line is on-hook as claimed in Claim 26 must be shown or the feature canceled from the claim. No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 25 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 25 recites the limitation "said electronic inductor transistor" in the 5th and 6th lines. There is insufficient antecedent basis for this limitation in the claim. The 3rd line recites the limitation "an electronic inductor". For the purpose of this Office action, to advance prosecution to the maximum degree possible, examiner makes prior art rejections based on the assumption that the recitation in the 3rd line is intended as "an electronic inductor transistor".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 18 through 22, 24, 25, 27 through 30 and 32 through 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiyoshi (US Patent 5,734,703).

6. Regarding Claim 18, Hiyoshi discloses a circuit for connecting a modem to a two-wire circuit (i.e., a telephone line) (Fig. 9, reference 540, 103; column 1, lines 16-20) comprising: a voltage controlled current source including an operational amplifier (Fig. 9, reference 540) having a positive input connected to a modem output driver (i.e., a transmit signal driver of the modem) (Fig. 9, reference 520; column 18, lines 3-4); the operational amplifier having an output driving the base of a transistor to form a semiconductor inductor circuit (i.e., an electronic inductor transistor) (Fig. 9, reference 540; column 18, lines 3-4); the transistor connected across

a rectified (Fig. 9, reference 103; column 18, line 5) two-wire circuit (i.e., tip and ring voltage of the telephone line).

7. Regarding Claim 19, Hiyoshi further discloses the negative input of the operational amplifier connected, via a resistor, to the transistor emitter (Fig. 9, reference 540).

8. Regarding Claim 20, Hiyoshi further discloses a resistor and capacitor forming a voltage divider connected to the positive input of the operational amplifier (Fig. 9, reference 540).

9. Regarding Claim 21, Hiyoshi further discloses a balancing bridge (i.e., impedance matching) circuit (Fig. 9, reference 11; column 9, lines 52-55) connected between the positive input of the operational amplifier and the collector of the transistor (Fig. 9, reference 540).

10. Regarding Claim 22, Hiyoshi further discloses a resistor connected between the operational amplifier positive input and the transistor emitter (i.e., to an emitter of the electronic inductor transistor) (Fig. 9, reference 540).

11. Regarding Claim 24, Hiyoshi further discloses a capacitor between the modem output driver (i.e., a transmit signal driver) and the positive input of the operational amplifier (Fig. 9, reference 520, 540).

12. Regarding Claim 25, Hiyoshi discloses a circuit for connecting a modem to a two-wire circuit (i.e., a telephone line) (Fig. 9, reference 540, 103; column 1, lines 16-20) comprising: an operational amplifier (Fig. 9, reference 540) having an output driving the base of a transistor to form a semiconductor inductor circuit (i.e., an electronic inductor transistor) (Fig. 9, reference 540; column 18, lines 3-4); and a hookswitch (Fig. 9, reference 550) connected between the two-wire circuit and the rectifier (Fig. 9, reference 103) and therefore, not connected between the rectified tip and ring voltage and the modem.

13. Regarding Claim 27, Hiyoshi further discloses the negative input of the operational amplifier connected, via a resistor, to the transistor emitter (Fig. 9, reference 540).

14. Regarding Claim 28, Hiyoshi further discloses a resistor and capacitor forming a voltage divider connected to the positive input of the operational amplifier (Fig. 9, reference 540).

15. Regarding Claim 29, Hiyoshi further discloses a balancing bridge (i.e., impedance matching) circuit (Fig. 9, reference 11; column 9, lines 52-55) connected between the positive input of the operational amplifier and the collector of the transistor (Fig. 9, reference 540).

16. Regarding Claim 30, Hiyoshi further discloses a resistor connected between the operational amplifier positive input and the transistor emitter (i.e., to an emitter of the electronic inductor transistor) (Fig. 9, reference 540).

17. Regarding Claim 32, Hiyoshi further discloses a capacitor between the modem output driver (i.e., a transmit signal driver) and the positive input of the operational amplifier (Fig. 9, reference 520, 540).

18. Regarding Claim 33, Hiyoshi discloses a circuit for connecting a modem to a two-wire circuit (i.e., a telephone line) (Fig. 9, reference 540, 103; column 1, lines 16-20) comprising: modem output driver (i.e., DC loop current) circuit (Fig. 9, reference 520: column 18, lines 3-4) having an operational amplifier (i.e., a first operational amplifier) having an output connected to the base of a transistor (i.e., a first electronic inductor transistor) connected across a rectified (Fig. 9, reference 103; column 18, line 5) two-wire circuit (i.e., tip and ring voltage of the telephone line) and a semiconductor inductor circuit (Fig. 9, reference 540; column 18, lines 3-4) (i.e., AC current circuit) having another operational amplifier (i.e., a second operational amplifier) having an output connected to the base of a transistor (i.e., a second electronic

inductor transistor) connected across a rectified (Fig. 9, reference 103; column 18, line 5) two-wire circuit (i.e., tip and ring voltage of the telephone line).

19. Regarding Claim 34, Hiyoshi further discloses a voltage divider comprising two resistors connected to the positive input of the operational amplifier in the modem output driver (i.e., DC loop current) circuit (i.e., the first operational amplifier) (Fig. 9, reference 520).

20. Regarding Claim 35, Hiyoshi further discloses resistors connected to the emitter of the transistor in the modem output driver (i.e., DC loop current) circuit (i.e., the first electronic inductor transistor) (Fig. 9, reference 520).

21. Regarding Claim 36, Hiyoshi further discloses the operational amplifier in the semiconductor inductor circuit (i.e., AC current circuit) (Fig. 9, reference 540) (i.e., the second operational amplifier) having a positive input connected to a modem output driver (i.e., a transmit signal driver of the modem) (Fig. 9, reference 520; column 18, lines 3-4).

22. Regarding Claim 37, Hiyoshi further discloses a balancing bridge (i.e., impedance matching) circuit (Fig. 9, reference 11; column 9, lines 52-55) connected between the positive input of the operational amplifier in the semiconductor inductor circuit (i.e., AC current circuit) (Fig. 9, reference 540) (i.e., the second operational amplifier) and the collector of the transistor in the semiconductor inductor circuit (i.e., AC current circuit) (i.e., the second electronic inductor transistor).

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 23 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiyoshi in view of Gay et al. (US Patent 4,796,295).

25. Regarding Claim 23, as shown above apropos of Claim 18, Hiyoshi anticipates all elements except a second transistor having a base connected to the collector of the electronic inductor transistor. Gay discloses a telephone interface circuit (Fig. 1) with a transistor (Fig. 1, reference 6) connected to the output of an operational amplifier (Fig. 1, reference 14) driven by an amplifier (Fig. 1, reference 18) that receives a transmit signal (Fig. 1, reference 20; column 3, lines 35-39). As such, the transistor (Fig. 1, reference 6) corresponds to the transistor in Hiyoshi, Fig. 9, reference 540 and to the electronic inductor transistor claimed. Gay further discloses another transistor (Fig. 1, reference 5) with a base connected to the collector of the first (i.e., electronic inductor) transistor. Gay discloses that by driving the second transistor in this way, line current is not drawn until the first (i.e., electronic inductor) transistor is active (column 4, lines 9-16). This avoids leakage currents that could result in the telephone line spuriously going into an off-hook state, especially when plural devices share a line. Therefore it would have been obvious to one skilled in the art at the time of the invention to apply the second transistor with a base connected to the collector of the first transistor as taught by Gay to the circuit taught by Hiyoshi for the purpose of reducing leakage currents and their undesirable effects.

26. Regarding Claim 31, as shown above apropos of Claim 25, Hiyoshi anticipates all elements except a second transistor having a base connected to the collector of the electronic inductor transistor. Gay discloses a telephone interface circuit (Fig. 1) with a transistor (Fig. 1,

reference 6) connected to the output of an operational amplifier (Fig. 1, reference 14) driven by an amplifier (Fig. 1, reference 18) that receives a transmit signal (Fig. 1, reference 20; column 3, lines 35-39). As such, the transistor (Fig. 1, reference 6) corresponds to the transistor in Hiyoshi, Fig. 9, reference 540 and to the electronic inductor transistor claimed. Gay further discloses another transistor (Fig. 1, reference 5) with a base connected to the collector of the first (i.e., electronic inductor) transistor. Gay discloses that by driving the second transistor in this way, line current is not drawn until the first (i.e., electronic inductor) transistor is active (column 4, lines 9-16). This avoids leakage currents that could result in the telephone line spuriously going into an off-hook state, especially when plural devices share a line. Therefore it would have been obvious to one skilled in the art at the time of the invention to apply the second transistor with a base connected to the collector of the first transistor as taught by Gay to the circuit taught by Hiyoshi for the purpose of reducing leakage currents and their undesirable effects.

27. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiyoshi in view of Horiuchi (US Patent 5,220,597).

28. Regarding Claim 26, as shown above apropos of Claim 25, Hiyoshi anticipates all elements except the base of the electronic inductor transistor being connected to ground when the telephone line is on-hook. Horiuchi discloses a circuit (Fig. 7) with a transistor (Fig. 7, reference 54) that drives a telephone line via a rectifier bridge and, as such, corresponds to the electronic inductor transistor claimed (Fig. 7, reference 50) and is maintained in an on-hook state by a circuit that grounds the transistor base (Fig. 7, reference 75; column 7, line 65 through column 8, line 3). Therefore it would have been obvious to one skilled in the art at the time of the

invention to apply base grounding in the on-hook state as taught by Horiuchi to the circuit taught by Hiyoshi for the purpose of avoiding spurious off-hook occurrences.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Swerdlow whose telephone number is 703-305-4088. The examiner can normally be reached on Monday through Friday between 8:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forrester Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel Swerdlow, Patent Examiner AU 2644